PREVENTION OF PARASITIC CHANNEL IN AN INTEGRATED SOI PROCESS

TECHNICAL FIELD

This invention relates to CMOS devices, and more specifically, to a technique of achieving elimination of the parasitic MOS channel present in thin film CMOS devices configured in the source, or what is called the source follower, configuration. Also disclosed is a methodology of performing a deep N implant in order to effectuate the inventive structure. Although most applicable in PMOS devices, the invention may also be utilized in the NMOS configuration.

BACKGROUND AND SUMMARY OF THE INVENTION

Figure 1 shows a thin film CMOS device including a source 101, drain 102, and MOS gate region 103. The SOI layer 104 forms an MOS junction 105 with an buried oxide layer 106. Below buried oxide layer 106 is a substrate layer 107, which would typically be several hundred microns thick. On the scale shown in Figure 1, the substrate layer 107 is too thick to depict and thus is not fully shown.

In source follower mode, sometimes called source high mode, the source 101 is biased with a voltage that is typically higher than the voltage at which substrate 107 is kept. This voltage difference could be over two hundred volts in typical applications. In thin film devices where the SOI layer 104 may be only slightly more than a micron thick, this voltage difference may be sufficient to induce an unwanted depletion region at or near the MOS junction 105. As shown therefore in Figure 1, a parasitic path 110 between source 101 and drain 102 exists at the MOS junction. This region creates a parasitic MOS channel, allowing leakage current to be conveyed between the source 101 and drain 101 when the real MOS gate region 103 is intended to be turned off. The device thus undesirably acts as if a second gate region existed, wherein the second gate is in the on state even when the actual gate region 103 is in the off state.

To date, there exists no known solution for stopping this leakage current when thin film SOI devices are utilized in the source follower configuration. Prior solutions all involve use of a much thicker SOI layer 104, rather than thin film devices. These prior devices have such a thick SOI layer that the depletion region resulting in the parasitic MOS channel 110 does not occur. However, in thin film applications the region 110 acts as a second current path in addition to the normal gate region.

There exists a need in the art for a technique of eliminating this parasitic channel 110 in source follower configurations with thin film SOI devices.

In complimentary arrangements, (i.e. using NMOS devices in which the source is biased much lower than the substrate) a similar problem may exist.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a depiction of a prior art CMOS thin film device, showing a parasitic MOS channel 110;

Figure 2 is a conceptual depiction of a device fabricated in accordance with the present invention; and

Figures 3A – D depict doping concentrations at various locations throughout the device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 2 depicts an exemplary PMOS device including the deep N layer 201 placed below the source region 101. A substrate region 107 is maintained at an exemplary voltage of –200, over 200 volts lower that the typical voltage at which the source is biased. Due to the relatively thin SOI layer 104, (slightly more than 1 micron) a parasitic MOS channel 110 results from a depletion region that forms between the drain 102 and source 101 as indicated in Figure 1. However, the deep N layer 201shown directly below the source region 101 prevents full depletion and instead forms the space charge neutral region 205 as indicated in dotted outline in Figure 2. This space charge neutral region205 prevents current flow between the source 101 and drain 102 along any parasitic channel than may otherwise be formed across MOS channel 110.

In the preferred embodiment, the implantation of the deep N layer 201 should be accomplished using a doubly ionized implant of 31P++ and a 200 KeV implant machine. This gives 400 KeV implant energy, without the need for a high energy implant machine.

It is also noted that while the deep N layer is shown below the source region 101 in Figure 2, it is noted that the space charge neutral region 205 may be implemented anywhere along what would otherwise be the parasitic current path 110 between the source 101 and drain 102. Thus, the deep N layer 201 may be placed directly below drain region 102, rather than below source region 101.

While the device has principal application in source high PMOS configurations, the complimentary device may be implemented in NMOS as well. Such an MMOS device would involve the P implant below the source or drain in similar concentration to those already described, and would be applicable in arrangements where the bias configuration of the device is the reverse of what has been described herein with respect to PMOS devices.

Figures 3A – D show further manufacturing information regarding the implementation of the present invention in a PMOS device. Fig. 3A depicts a cross section showing the relative thickness' of the various portions of the device previously described. The device depicted in 3A is doped in concentrations profiled in Figure 3B. Note that Figures 3C and 3D compare the doping concentrations present in the source and drain regions respectfully. Note the concentration of the doping in the deep N region is shown is Figure 3D as being approximately 1 order of magnitude higher than the concentration shown in Figure 3B for the Nwell, the gate region.

It is noted that while the above describes the preferred embodiment of implementing the invention, various modifications and additions will be apparent for those that are skilled in the art. Such modifications are intended to be covered by the claims appended hereto.)